WHAT IS CLAIMED IS:

1. A method of manufacturing a Metal Oxide Semiconductor (MOS) transistor, comprising:

forming an active area in a substrate, wherein said active area is bounded by an isolation structure; and

placing at least one stress adjustor adjacent said active area, wherein said stress adjustor is positioned to modify a mobility of a majority carrier within a channel region of said MOS transistor.

2. The method as recited in Claim 11, wherein placing said stress adjustor includes removing portions of said silicon substrate to form at least two trenches and filling said trenches with a material comprising said isolation structure.

3. The method as recited in Claim 1, wherein placing said stress adjustor includes removing a portion of said isolation structure to form a trench and filling said trench with an insulator.

4. The method as recited in Claim 3, wherein filling said trench with said insulator includes a high density plasma oxide deposition.

5. The method as recited in Claim 3, wherein filling said trench with said insulator includes a spin-on-glass type oxide.

6. The method as recited in Claim 1, wherein said stress adjustor is configured to decrease a compressive stress imparted from said isolation structure to said channel region.

7. The method as recited in Claim 1, wherein said stress adjustor is configured to increase a compressive stress imparted from said isolation structure to said channel region.

8. A Metal Oxide Semiconductor (MOS) transistor, comprising:

an active area in a substrate;

an isolation structure in said substrate and surrounding said active area; and

at least one stress adjustor adjacent said active area, wherein said stress adjustor is positioned to modify a mobility of a majority carrier within a channel region of said MOS transistor.

9. The MOS transistor recited in Claim 8, wherein a long dimension of said stress adjustor is perpendicular to an intended direction of current flow and said long dimension has length substantially equal to a gate width of said MOS transistor.

10. The MOS transistor recited in Claim 8, wherein a long dimension of said stress adjustor is parallel to an intended direction of current flow and said long dimension has a length substantially equal to a gate length of said MOS transistor.

11. The MOS transistor recited in Claim 8, wherein a portion of said isolation structure is between said active area and said stress adjustor.

12. The MOS transistor recited in Claim 8, wherein a distance between a perimeter of said stress adjustor and a perimeter of said active area is at least about 50 nanometers.

13. The MOS transistor recited in Claim 8, wherein said stress adjustor comprises a portion of said silicon substrate.

14. The MOS transistor recited in Claim 8, wherein said stress adjustor comprises silicon oxide.

15. The MOS transistor recited in Claim 8, wherein said MOS transistor is an NMOS transistor and said stress adjustor reduces a compressive stress to a channel of said NMOS transistor.

16. The MOS transistor recited in Claim 15, wherein said NMOS transistor has an active overlap of about 500 nanometers or less.

17. The MOS transistor recited in Claim 8, wherein said MOS transistor is a PMOS transistor and said stress adjustor enhances a compressive stress to a channel of said PMOS transistor.

18. A process for constructing an integrated circuit (IC), including:

generating a mask layout for an IC, comprising:

calculating an active overlap distance between a planned perimeter of a gate of said IC and a planned perimeter of an active area of said IC;

determining a compressive stress along a direction of an intended current flow through a planned channel of said IC based on said active overlap distance; and

introducing a stress adjustor area adjacent said active area to modify a mobility of a majority carrier through said planned channel, if said compressive stress is greater than a critical stress parameter; and

using said mask layout to produce said IC.

19. The method of Claim 18, wherein said critical stress parameter is adjusted to different values depending on whether said mask layout data set defines an NMOS or a PMOS transistor.

20. The method of Claim 18, wherein said critical stress parameter corresponds to a predefined active overlap distance.